UNIVERSITÀ
DI PAVIA

Dipartimento di Ingegneria Industriale e dell'Informazione

AVVISO DI SELEZIONE PER IL PROGETTO "LAUREE MAGISTRALI PLUS"
CORSO DI LAUREA ELECTRONIC ENINEERING

COORTE MATRICOLE LM A.A. 2017/2018

ANNO ACCADEMICO DI SVOLGIMENTO DELL'ESPERIENZA IN AZIENDA
2018/2019 (SECONDO SEMESTRE dell'A.A.)

Art. 1 – Selezione
Nell'ambito del Progetto Laurea Magistrale Plus (di seguito "LM+") promosso dall'Università degli Studi di Pavia in convenzione con le Imprese interessate, è indetta la presente selezione (di seguito anche "avviso" o "bando") finalizzata all'individuazione di studenti interessati allo svolgimento di un'esperienza in azienda allo scopo di integrare le competenze acquisite nell'ambito dei loro percorsi di studio.
Tale esperienza sarà effettuata nell'arco temporale di massimi 12 mesi, in taluni casi suddivisi in due (2) periodi di sei (6) mesi, come specificato nei progetti proposti.
Il presente avviso è riservato agli studenti iscritti al corso di laurea magistrale in Electronic Engineering.

Eventuali ulteriori informazioni relative alle finalità di ciascun Progetto e alle modalità di partecipazione possono essere richieste al Docente del corso di laurea Referente per il progetto LM+ di seguito indicato:
Prof. Sabina Merlo
Referente per il Progetto LM+ del corso di laurea magistrale in Electronic Engineering
e-mail: sabina.merlo@unipv.it
tel. 0382985202

I progetti di tirocinio presentati dalle aziende partner del progetto costituiscono parte integrante del presente bando (Allegato A).

Art. 2 – Requisiti di ammissione
Sono ammessi a partecipare alla presente selezione coloro che, alla data di scadenza del bando, risultano studenti regolarmente iscritti al primo anno di Laurea Magistrale (LM) dell'Università degli Studi di Pavia in Electronic Engineering

Art. 3 – Procedure per accedere alla selezione
Ai fini della selezione ciascun candidato dovrà candidarsi tramite la compilazione del form online disponibile sul sito http://cor.unipv.eu/site/home.html alla voce **"Avvisi di selezione Lauree Magistrali Plus - studenti immatricolati a.a. 2017-2018".**
Ciascuno studente accede all'applicativo "progetti COR" individua il proprio corso di laurea, si registra, seleziona le proposte delle aziende di suo interesse, allega il suo Curriculum Vitae (formato word e pdf) e conferma la sua candidatura.
Gli studenti devono indicare le proprie preferenze per n. 3 progetti proposti dalle aziende.

È possibile candidarsi al progetto fino alle ore 24.00 del giorno 31 luglio 2018.
I dati personali trasmessi dai candidati con le domande di partecipazione al bando sono raccolti presso l'Università degli Studi di Pavia, Titolare del trattamento, nel rispetto delle condizioni di liceità (art. 6 par. 1 Regolamento UE 2016/679) saranno trattati da soggetti autorizzati dal Titolare del trattamento in relazione alle loro funzioni e competenze per le finalità di gestione della procedura di selezione. Per le stesse finalità i dati potranno essere comunicati alle aziende partner del progetto. Per esercitare i diritti sui propri dati personali previsti dalla normativa rivolgersi al Titolare. L'informativa completa relativa al trattamento dei dati personali è disponibile al link http://privacy.unipv.it/

Art. 4 – Procedura di selezione dei partecipanti
Il Consiglio didattico del corso di laurea magistrale in Electronic Engineering ha nominato in data 16 aprile

2018 una commissione giudicatrice composta da n. 7 docenti.
I docenti sono:
- Sabina Merlo, Presidente
- Antonio Agnesi, membro della Commissione
- Fabio Dell'Acqua, membro della Commissione
- Lorenzo Favalli, membro della Commissione
- Piero Malcovati, membro della Commissione
- Andrea Mazzanti, membro della Commissione
- Pietro Savazzi, membro della Commissione

La selezione verrà essere effettuata in presenza di almeno 3 membri della Commissione.

Il Presidente della Commissione è il docente referente del corso di laurea per il progetto LM+. I docenti membri della commissione giudicatrice assegneranno autonomamente il ruolo di Segretario a un docente della Commissione.

La Commissione, nel rispetto dei criteri di selezione di seguito riportati, procederà alla valutazione delle candidature e all'individuazione di un elenco di candidati che saranno convocati ad un colloquio alla presenza delle aziende partner che hanno formalizzato le proposte di tirocinio. La Commissione acquisirà dai referenti aziendali parere non vincolante finalizzato alla scelta dei candidati.
L'elenco dei candidati convocati per il colloquio con la Commissione, che si terrà il 13 settembre 2018 presso i locali del Dipartimento di Ingegneria Industriale e dell'Informazione, Via Ferrata 5, 27100 Pavia, sarà pubblicato sulle pagine web della Facoltà di Ingegneria (http://webing.unipv.eu) unitamente all'ora e luogo della convocazione stessa. Gli studenti convocati a colloquio riceveranno comunicazione anche tramite posta elettronica.
La pubblicazione sul web, unitamente alla comunicazione tramite posta elettronica, esaurisce l'obbligo di notifica da parte dell'Università di Pavia nei confronti dei candidati che, pertanto, dovranno verificare gli orari e il luogo dove si svolgeranno i colloqui consultando regolarmente il sito web innanzi indicato e la casella di posta elettronica di Ateneo.

La Commissione di docenti procederà alla selezione degli studenti e all'abbinamento azienda/studente sulla base delle indicazioni aziendali e in considerazione delle preferenze espresse dagli studenti.

Art. 5 – Le proposte di tirocinio delle aziende partner
Le proposte avanzate dalle aziende per lo svolgimento dell'esperienza di tirocinio riservata agli studenti del corso di laurea magistrale in Electronic Engineering sono:

- **Bright Solutions**: "Solid State Lasers"
- **CEA-LETI**: "Analysis and RFIC design of THz oscillator"
- **eSilicon**: "High Speed Serial Interface for Data Center Application: Mixed signal simulations, full validation and automated standard compliance test"
- **GENEGIS GI**: "PULSE urban sensor systems"
- **Infineon technologies**: "Modelling of power management for autonomous driving"
- **Prisma Telecom Testing**: "Integration and verification of testing hw/sw for 4g/5g radio access network performance assessment"
- **STMicroelectronics**: "Innovative approaches for low power, high performance MEMS products"
- **STMicroelectronics**: "Analog design for Power Combo"
- **STMicroelectronics**: "Electro-optical signal conditioning architectures based on Silicon Photonics technology"
- **TIM-ITALTEL**: "Software Defined Optical Networks - Softwarized Network Control Layer"

Il contenuto delle proposte, dettagliato con le attività, è riportato in allegato al bando sotto la lettera A, per formarne parte integrante e sostanziale.

Art. 6 – Criteri di selezione

La selezione si svolge per titoli e colloquio.
I criteri di valutazione per l'assegnazione del punteggio a ciascun candidato sono i seguenti:

1. **VALUTAZIONE DELLA DOCUMENTAZIONE**, per accertare:
   - l'esistenza dei requisiti formali di ammissione previsti;
   - il rispetto dei termini per la presentazione della candidatura.
2. **VALUTAZIONE DEL MERITO**
   - Numero di CFU acquisti per gli insegnamenti del primo anno accademico della Laurea Magistrale: 1 punto ogni 3 CFU acquisiti.
   - Votazione media per gli esami sostenuti nel primo anno accademico della Laurea Magistrale, fino a un massimo di 10 punti secondo la tabella di seguito riportata:
     - fino a 21/30 0 punti;
     - fino a 25/30 2 punti;
     - fino a 28/30 6 punti;
     - fino a 30/30 10 punti.

     La Commissione docenti verificherà il numero di CFU e votazione media di ciascuno dei candidati dopo la chiusura del bando, attraverso i database di Ateneo di gestione delle carriere studenti. Non è richiesta agli studenti alcuna autocertificazione di questi dati.
3. **VALUTAZIONE DI ALTRI TITOLI**
   Sono, altresì, sottoposti alla valutazione della Commissione, con l'attribuzione di un punteggio fino a un massimo di 10:
   - il Curriculum Vitae;
   - altre esperienze attinenti e propedeutiche ed eventuali certificazioni (es. certificazioni linguistiche).
4. **COLLOQUIO INDIVIDUALE**
   Il colloquio individuale, a cui è attribuito un punteggio fino a un massimo di 20, è volto ad accertare:
   - le motivazioni e le aspettative espresse e argomentate dallo studente in questa sede;
   - la curiosità scientifica manifestata.

   A discrezione della Commissione sarà possibile convocare a colloquio una frazione di candidati, comunque non inferiore al 50% di quanti hanno fatto domanda, sulla base della graduatoria di cui sopra risultante dalla valutazione del merito e di altri titoli.

Art. 7 – Pubblicazione della graduatoria

Entro il 5 ottobre 2018 sarà pubblicata sull'Albo Ufficiale e sul sito della **Facoltà di Ingegneria (http://webing.unipv.eu)** la graduatoria dei candidati selezionati dalla Commissione dei docenti. La graduatoria prevede anche l'indicazione dell'abbinamento studente con l'azienda/progetto di tirocinio per i vincitori. La Commissione dei docenti può riservarsi di non assegnare tutti i progetti presentati dalle aziende.

Art. 8 – Modalità di accettazione del progetto

I candidati assegnati a ciascun progetto dovranno presentarsi nel periodo 8-12 ottobre 2018 presso la Segreteria del **Dipartimento di Ingegneria Industriale e dell'Informazione, piano F, Via Ferrata 5, 27100 Pavia** dalle ore 9:30 alle ore 12:00 per firmare l'atto di accettazione del Progetto.
In caso di mancata presentazione del modulo di accettazione, il candidato decadrà dall'assegnazione del progetto stesso. In caso di rinuncia del candidato selezionato, verranno contattati i candidati risultati idonei secondo la lista di assegnazione individuata dalla Commissione, ai sensi del precedente art. 7.

Art. 9 – Caratteristiche del tirocinio

Per le modalità e finalità del progetto LM+ definite nella convenzione tra Ateneo e Azienda, l'esperienza in azienda di ciascun studente selezionato si realizzerà attraverso l'istituto del tirocinio formativo curriculare.
L'Università degli Studi di Pavia, in qualità di soggetto promotore assicura il tirocinante contro gli infortuni sul lavoro presso l'INAIL, nonché presso idonee compagnie assicuratrici per la responsabilità civile verso terzi e per l'infortunio.
Per le attività di tirocinio ciascuna azienda corrisponde direttamente al tirocinante una somma pari ad almeno 500,00 euro lordi mensili a titolo di rimborso spese forfettario. L'importo indicato nell'ambito di ciascun tirocinio è esplicitato in ciascuna proposta di tirocinio delle aziende partner di cui all'allegato A, comprensiva dell'indicazione di eventuali altri benefit previsti dall'azienda.
Il tirocinio formativo non costituisce in alcun modo rapporto di lavoro.

Art. 10 – Durata del tirocinio
Tenuto conto di quanto indicato all'art. 1, le attività di tirocinio si svolgeranno con data di inizio a partire dai primi tre mesi del 2019, per una durata massima di 12 mesi.
La data di avvio del tirocinio sarà concordata direttamente da ciascuna azienda con il candidato selezionato e il relativo tutor universitario e sarà riportata nel progetto formativo.

Art. 11 – Eventuale modifica del regime di iscrizione ai corsi di laurea magistrale, da tempo pieno a tempo parziale
Ciascun studente che risulti vincitore di una proposta di tirocinio ha facoltà di modificare il proprio regime di iscrizione al corso di laurea da tempo pieno a tempo parziale, come disciplinato dal *Regolamento per l'iscrizione in regime di tempo parziale* emanato dall'Università degli Studi di Pavia con Decreto Rettorale n. 818/2013 del 15 maggio 2013.

Art. 12 – Riservatezza
Il livello di riservatezza delle informazioni aziendali di cui verranno a conoscenza il tirocinante e il tutor universitario è definito nella convenzione stipulata tra l'Università degli Studi di Pavia e ciascuna azienda e potrà, altresì, essere ulteriormente disciplinato da specifici patti di riservatezza che l'azienda farà sottoscrivere al tirocinante e al tutor universitario.
Tale principio trova applicazione anche in riferimento ai contenuti della tesi elaborata dallo studente, se concernente tematiche attinenti alle attività aziendali e alle nozioni acquisite durante il tirocinio.

Art. 13 – Formazione sulla sicurezza
Ai sensi dell'art. 2 comma 1 lett. a) del D.Lgs. 81/08 "Testo Unico sulla salute e sicurezza sul lavoro", i vincitori della selezione dovranno partecipare alla formazione generale sulla sicurezza e alla formazione specifica concernente i rischi a cui i tirocinanti saranno esposti all'interno dell'azienda ospitante. Tale formazione sarà curata ed erogata dall'azienda ospitante.

Pavia, - 4 LUG 2018

È allegato al presente avviso di selezione, quale sua parte integrante:
Allegato A – progetti di tirocinio presentati dalle aziende partner per il Corso di Laurea Magistrale in Electronic Engineering

IL DIRETTORE DEL DIPARTIMENTO
Prof. Paolo Arcioni

UNIVERSITA' DEGLI STUDI DI PAVIA
DIP. INGEGNERIA INDUSTRIALE E DELL'INFORMAZIONE

IL DOCENTE REFERENTE PROGETTO LM+
Prof. Sabina Merlo

(Allegato A) - progetti di tirocinio presentati dalle aziende partner del progetto LM+

Le proposte avanzate dalle aziende per lo svolgimento dell'esperienza di tirocinio riservata agli studenti del corso di laurea in **Electronic Engineering** sono:

- ***Bright Solutions**: "Solid State Lasers"*
- ***CEA-LETI**: "Analysis and RFIC design of THz oscillator"*
- ***eSilicon**: "High Speed Serial Interface for Data Center Application: Mixed signal simulations, full validation and automated standard compliance test"*
- ***GENEGIS GI**: "PULSE urban sensor systems"*
- ***Infineon technologies**: "Modelling of power management for autonomous driving"*
- ***Prisma Telecom Testing**: "Integration and verification of testing hw/sw for 4g/5g radio access network performance assessment"*
- ***STMicroelectronics**: "Innovative approaches for low power, high performance MEMS products"*
- ***STMicroelectronics**: "Analog design for Power Combo"*
- ***STMicroelectronics**: "Electro-optical signal conditioning architectures based on Silicon Photonics technology"*
- ***TIM-ITALTEL**: "Software Defined Optical Networks - Softwarized Network Control Layer"*

Unipv LM+

Progetto Laurea Magistrale Plus

(Students enrolled for the first time in the Academic Year 2017/18, undertaking the internship in the company in 2018/19)

University infos

Laurea degree - LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING
University tutor / Thesis supervisor - Prof. Antoniangelo Agnesi
Courses / Expertize of the university tutor - Industrial Laser Design / Laser sources, nonlinear optics, industrial photonics

Company infos

Company name - Bright Solutions
Company Tutor(s) - Stefano Dell'Acqua
Role in the company of the tutor(s) - R&D Project Manager

Contents and infos on project and internship

Project title: Solid State Lasers
Activity scenario and targets of the internship - Area/Department/office/lab (where the trainee will be involved) The candidate will be guided in developing specific knowledge, both theoretical and experimental, in design and realisation of laser sources and systems based on DPSS (Diode Pumped Solid State) technology. Realisation and detailed characterisation of a high-peak power pulsed DPSS laser system will be the main task. Collaboration with highly qualified professionals as well as training-on-the-job, will offer an effective way to assess the progress of field knowledge and technical skill of the candidate, including his ability in using laboratory equipment.
Background / Expertize of the student required for the internship Knowledge of principles of modern photonics, electronics and computer science technologies at Master degree level; practical experience of photonics laboratories preferred (e.g. Master thesis)
Potential thesis topics **Solid-state Lasers** / Design, realization and characterization of a DPSS laser with high peak power
Company location and place of work Design and development - Bright Solutions Srl - Via Artigiani 27 Cura Carpignano (PV)
Time length of the internship 12 MONTHS
Benefits provided by the company (at least reimbursement of 500€ per month) Monthly allowance 500 Euro + Ticket restaurant
Specific company requests Strongly motivated individuals, with manual/laboratory skills, good exams score and pertinent study curriculum
Other comments

Progetto Laurea Magistrale Plus

(Students enrolled for the first time in the Academic Year 2017/18, undertaking the internship in the company in 2018/19)

University infos

Laurea degree LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING
University tutor / Thesis supervisor - ANDREA MAZZANTI
Courses / Expertize of the university tutor Circuits & Systems for High Speed Communications / Industrial Topics in Microelecronics. The research interests of the academic tutor are focused on the design of integrated circuits for ultra-high speed wireless and wireline communication systems.

Company infos

Company name CEA-LETI
Company Tutor - Dr. Jose Luis GONZALEZ-JIMENEZ Phone : +33 438 78 33 58 E-mail : joseluis.gonzalezjimenez@cea.fr
Role in the company of the tutor(s) - Research-engineer, senior expert

Contents and infos on project and internship

Project title - Analysis and RFIC design of THz oscillator
Activity scenario and targets of the internship - Area/Department/office/lab (where the trainee will be involved): The student will integrate the RFIC design laboratory of the Integrated Circuits, Systems and Architectures Dpeartment of LETI, the Information Technology and Electronics Research Institute of the CEA in Grenoble, France. The RFIC lab is composed by 20 permanent reserach engineers and 20 non-permanent staff (Ms.S, Ph.D, Post-Doc). The RFIC laboratory performs research and development in close contact with industry and in collaboration with other research centers and universities in the files of low power and UWB RFIC design, devices and circutis for IoT applications, high-speed wirless communications in mmW and THz bands, front-end modules for cellular networks and WiFi, and advanced processign architectures for agile radio, radar and localization. The proposed intership is in the area of high-speed wirless communications in mmW and THz bands. The student will integrate the team of designers working in mmW IC design. He will participate fully in the laboratory activities and will have access to all the first grade design and simulation tools available in the laboratory, both for system level design (Matlab/Simulink) and for circuit design (Cadence/Eldo/Spectre/AMS).
Background / Expertize of the student required for the internship: Radio Frequency cicuits and systems Microelectronics, Integrated Circuits design techniques and tolls
Potential thesis topics: The stage will contribute to a larger study on novel architectures for wireless high-data rate transceivers designed using advanced CMOS technologies operating at THz frqeuencies. The student will be in charge of the study and design of one fundamental block of the emitter, specifically, of mmW LO generator based on advanced oscillators topologies. The outcome of this study may lead to the design of an integrated circuit in advanced technology node (FDSOI or PDSOI CMOS) that would be fabricated in a later stage.
Company location and place of work: CEA-LETI DRT/DACLE/SCCI/LAIR Building 52B MINATEC CAMPUS 17 rue des Martyrs, 38054 Grenoble CEDEX 9
Time length of the internship - 6 + 6 MONTHS
Benefits provided by the company (at least reimbursement of 500€ per month): 700€ stipend (brute) + 229€ possible aid for housing, if the conditions are fullfilled and all documents are provided.
Specific company requests - No specific company requests
Other comments

Unipv LM+

Progetto Laurea Magistrale Plus

(Students enrolled for the first time in the Academic Year 2017/18, undertaking the internship in the company in 2018/19)

University infos

Laurea degree LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING
University tutor / Thesis supervisor - Andrea Mazzanti
Courses / Expertize of the university tutor Circuits & Systems for High Speed Communications / Industrial Topics in Microelecronics. The research interests of the academic tutor are focused on the design of integrated circuits for ultra-high speed wireless and wireline communication systems.

Company infos

Company name eSilicon Italy s.r.l.
Company Tutor(s) Matteo Pisati - Roberto Massolini
Role in the company of the tutor(s) Staff Analog Design Engineer/ Staff Hardware Engineer

Contents and infos on project and internship

Project title - High Speed Serial Interface for Data Center Application: Mixed signal simulations, full validation and automated standard compliance test
Activity scenario and targets of the internship - Area/Department/office/lab (where the trainee will be involved) The candidate will have the opportunity to choose between two types of mutually exclusive activities. **The first option is a design and mixed-mode circuit simulation activity.** The candidate will work in close contact with the system architects, analog and digital designers to simulate and verify the functionality and the performance of top level blocks of a High speed Serial Interface (SerDes). The candidate will be exposed to state of the art high speed serial interface design and will help to validate the circuit functionality and benchmark it against the model to help verifying that the schematic design meets the electrical specifications defined by the system architects. The circuits that the candidate will deal with include: Continuous Linear Equalizers, Multi GHz VCO, fractional PLL, ADC, DAC, Band Gap, voltage/current reference and temperature sensors. **The second option is related to measurement and validation activities done in the lab on real silicon devices**. The candidate will work in close contact with the system architects, analog and digital designers, firmware and hardware engineer to test the functionality and the performance of top level blocks of a High Speed Serial Interface (SerDes). The candidate will be exposed to state of the art high speed serial interface design and will help to test the circuit functionality and performance as well automate compliance tests specific to the standard. The candidate will use specific instrumentation and will design software to build Virtual Instruments that control the device under test.
Background / Expertize of the student required for the internship Good knowledge of electronics Able to work in a team Good communication skill Good spoken and written English
Potential thesis topics: Top level verification of 112GSps PAM4 SerDes blocks
Company location and place of work: Viale della Repubblica 38, 27100 Pavia Italy
Time length of the internship: 12 MONTHS
Benefits provided by the company (at least reimbursement of 500€ per month) Reimboursment 500€ per month + 7.5€ Ticket restaurant
Specific company requests
Other comments

Unipv LM+

Progetto Laurea Magistrale Plus

(Students enrolled for the first time in the Academic Year 2017/18, undertaking the internship in the company in 2018/19)

University infos

Laurea degree - LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING
University tutor / Thesis supervisor: Fabio Dell'Acqua
Courses / Expertize of the university tutor: Remote sensing, Earth observation

Company infos

Company name - GENEGIS GI SRL
Company Tutor(s) - Francesca Sapio
Role in the company of the tutor(s): rRsearch and Innovation manager

Contents and infos on project and internship

Project title - PULSE urban sensor systems
Activity scenario and targets of the internship - Area/Department/office/lab (where the trainee will be involved) The proposed stage is included in an European project in progress Pulse . The activities of this project are developed in collaboration with Prof. Gamba, for remote sensing and EO aspects, and Prof. Casella, for the GIS part. The core of the stagier project is to integrate data from city systems (health, environment, transport, planning) with data obtained via remote sensing (satellites and UAVs) and citizens (via apps and social media) to define the levels of generalized risk (health and safety) and resilience (the capacity of local resources to support individual and community health) in specific neighborhoods across the five cities (Paris, New York, Birmingham, Singapore, Barcelona) . New research in the field of exposomics aimed at modelling the impact of climate conditions and air quality on human health using remote sensing and mobile sensing technologies. Development of the PULSE integrated data ecosystem based on mobile devices (smart phones), sensor systems (remote sensing, including satellites and UAVs; fixed and mobile sensors) to enable large scale collection of citizen data within the smart city environment. PULSE will use satellites to assess and model air pollution. This technology, and associated analytics, is based on the inverse relationship between the thermal band recorded by space-borne sensors and the amount of pollution in the air. Specifically, the approach is based on the fact that air composition and characterization can be derived from satellite observations by the appropriate employment of algorithms that address the interaction between the physical effects of pollution and the soil radiance/irradiance recorded by the sensors. Pollution layers are the direct cause of a decrease of the atmospheric transmission factor at the infrared wavelengths. This effect impacts acquisitions in the thermal infrared band, as the solar heating is more affected than other wavelengths. Consequently, the sun-emitted radiance at the Earth surface appears lower than expected, and the signal reflected in any direction is lower in absolute value. Simultaneously, the pollution layer absorbs the reflected or emitted radiance, i.e., causes a pronounced loss of energy radiated upward. Hence, this physical process contributes to, and explains, the correlation between the increase in pollution and the decrease in apparent surface temperature as extracted from the thermal infrared records by airborne/satellite sensors. To evaluate this correlation, data from satellites and measurements on the ground are correlated, allowing for the detection of changes in pollution intensity at fine resolution and in a wide geographical area. The PULSE project will utilize the NASA and ESA satellites (i.e., Landsat-8) and ESA (i.e., Sentinel-2) in order to define and create dynamic maps of urban air quality using satellite imagery. The stagier project will apply the methodology developed during the PULSE project also to the Pavia municipality as a new test site actually not included the original European project.
Background / Expertize of the student required for the internship Good English/ previous knowledge of Python and SW GRASS.
Potential thesis topics General topic: earth observation and environmental monitoring Theme: integration among general environmental data regarding the urban system (health, environment, transport and planification information) and the data deduced by the remote sensing images.
Company location and place of work - Via Scarampo 47 - 20148 Milan
Time length of the internship - 12 MONTHS
Benefits provided by the company (at least reimbursement of 500€ per month) reimbursement of 500€ per month
Specific company requests
Other comments

Unipv LM+

Progetto Laurea Magistrale Plus

(Students enrolled for the first time in the Academic Year 2017/18, undertaking the internship in the company in 2018/19)

University infos

Laurea degree LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING
University tutor / Thesis supervisor - Piero Malcovati
Courses of the university tutor: Industrial Measurements, Electrical Industrial Measurements, Microsensors, Integrated Microsystems and MEMS Competences of the university tutor: Analog and mixed-signal integrated circuits, Sensor interface circuits, Data converters, Power electronics and power management

Company infos

Company name - Infineon Technologies
Company Tutor - Daniele Miatton
Role in the company of the tutor - Senior Expert Product Engineer

Contents and infos on project and internship

Project title - **Modelling of power management for autonomous driving**
Activity scenario and targets of the internship - Area/Department/office/lab (where the trainee will be involved) Automotive, Power Supply. Modelling power management for automotive electronics, especially for autonomous driving applications. Modeling SW usage and benchmarking in lab with a real device. Activity will be developed at Pavia office with possible travels to other Infineon offices within UE for short periods.
Background / Expertize of the student required for the internship Knowledge of analog electronics, modeling language and tools (e.g. Matlab) is a plus
Potential thesis topics Mathematical and behavioral modelling of intelligent power management devices for autonomous driving cars. Model fitting with experimental validation of the Silicon solution in the laboratory and with transistor level simulations.
Company location and place of work Infineon Technologies, Via Trieste 71, 27100 Pavia
Time length of the internship 12 MONTHS
Benefits provided by the company (at least reimbursement of 500€ per month) 800€ per month + 8€ ticket restaurant per day
Specific company requests - Availability to travel in Europe
Other comments

Unipv LM+

Progetto Laurea Magistrale Plus

(Students enrolled for the first time in the Academic Year 2017/18, undertaking the internship in the company in 2018/19)

University infos

Laurea degree LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING
University tutor / Thesis supervisor PIETRO SAVAZZI
Courses / Expertize of the university tutor Digital Signal Processing/Wireless Communication Systems

Company infos

Company name PRISMA TELECOM TESTING SRL
Company Tutor(s) PAOLO TIMELLI
Role in the company of the tutor(s) TEAM LEADER SYSTEM INTEGRATION & VERIFICATION DEPT.

Contents and infos on project and internship

Project title INTEGRATION AND VERIFICATION OF TESTING HW/SW FOR 4G/5G RADIO ACCESS NETWORK PERFORMANCE ASSESSMENT
Activity scenario and targets of the internship - Area/Department/office/lab (where the trainee will be involved) ACTIVITY: PERFORMANCE ASSESSMENT OF DEVICE UNDER TEST PERFORMANCES BY MEANS OF SPECIFIC TRAFFIC MODELS, REPORTING AND TESTING AUTOMATION SETUP – DEPT: HARDWARE & SOFTWARE INTEGRATION & VERIFICATION
Background / Expertize of the student required for the internship - MOBILE NETWORKS - PROTOCOLS & STANDARDS - SOFTWARE DEVELOPMENT - RADIO PROPAGATION
Potential thesis topics TRAFFIC MODEL DEFINITION IN ORDER TO ASSESS THE PERFORMANCE OF 4G/5G RAN (RADIO ACCES NETWORKS)
Company location and place of work VIA PETROCCHI 4, 20127 MILAN, Italy
Time length of the internship 12 MONTHS
Benefits provided by the company (at least reimbursement of 500€ per month) 700,00 EUROS + MENSA
Specific company requests
Other comments

Unipv LM+

Progetto Laurea Magistrale Plus

(Students enrolled for the first time in the Academic Year 2017/18, undertaking the internship in the company in 2018/19)

University infos

Laurea degree: LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING
University tutor / Thesis supervisor: Edoardo Bonizzoni
Courses / Expertize of the university tutor Courses: Analog Integrated Circuits, Elettronica 1 Expertise: design and characterization of analog circuits (high precision amplifiers, voltage references), analog-to-digital converters (both Nyquist rate and oversampled), DC-DC converters (single or multiple outputs), and sensor interfaces.

Company infos

Company name: STMicroelectronics
Company Tutor(s): Stefano Facchinetti / Andrea Donadel
Role in the company of the tutor(s): Analog IC Designer / Team Leader of Analog Design Team

Contents and infos on project and internship

Project title: Innovative approaches for low power, high performance MEMS products
Activity scenario and targets of the internship - Area/Department/office/lab (where the trainee will be involved): The intern will carry out feasibility studies for new architectural solutions for high performance MEMS devices, in particular 6x inertial modules. The internship activity will consist of an initial phase of literature review to identify state-of-the-art solutions. Once an effective solution is identified, the intern will model it in Matlab / Simulink to clearly identify the trade-offs and advantages / drawbacks. Finally, the solution will be implemented in Cadence (schematic level design) and simulated to validate the solution in ST technology. In coordination with the layout team, the design will be put in a test chip for final characterization at bench level (if feasible within the internship time span). Product Development group within the Analog, MEMS and Sensors (AMS) Division.
Background / Expertize of the student required for the internship: Strong understanding of integrated analog circuit design; understanding of the implications on the layout of design choices.
Potential thesis topics: Innovative approaches and architectures towards low power and high performance MEMS devices.
Company location and place of work: Via Tolomeo, 1 20010 Cornaredo (Mi), Italy.
Time length of the internship: 12 MONTHS
Benefits provided by the company (at least reimbursement of 500€ per month): Reimbursement: 600€ per month; ST shuttle service to reach the place of work; Lunch included at the ST canteen.
Specific company requests:
Other comments:

Unipv LM+

Progetto Laurea Magistrale Plus

(Students enrolled for the first time in the Academic Year 2017/18, undertaking the internship in the company in 2018/19)

University infos

Laurea degree LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING
University tutor / Thesis supervisor - Daniele Bajoni
Courses / Expertize of the university tutor Daniele Bajoni teaches Electromagnetism (Fisica 2) to undergraduate engineering students and "Introduction to Quantum Mechanics and Quantum Technologies" for master students in microelectronic engineering. His research is focused on integrated silicon photonics, in particular on the use of resonators to amplify optical nonlinearities and quantum effects in silicon devices.

Company infos

Company name STMicroelectronics
Company Tutor(s) Antonio Fincato
Role in the company of the tutor(s) Silicon Photonics Advanced R&D

Contents and infos on project and internship

Project title **Electro-optical signal conditioning architectures based on Silicon Photonics technology**
Activity scenario and targets of the internship - Area/Department/office/lab (where the intern will be involved) The activity involves the modeling of active electro-optical components such as optical phase shifters, modulators and switches based on ring resonators or Mach-Zehnder interferometers, as well as complex photonic architectures for sensor and / or telecom applications. The goal is to develop mathematical and behavioral models to be used in optical simulators (Lumerical, Optsim) and / or numerical computational environments (Matlab). It may be required that part of the internship be devoted to characterization. The intern will be included in a design team specialized in electro-optical structures in silicon photonics. The activity carried out may lead to the publication of articles at conferences or in international journals.
Background / Expertize of the student required for the internship Basic knowledge in photonics, electronics and semiconductor physics. It is also required familiarity and, possibly, experience in the use of numerical computing environments (Matlab) and / or optical simulators (Lumerical, Optsim). In case the internship project foresees laboratory measurements on prototypes, laboratory experience and / or aptitude for the experimental activities is appreciated.
Potential thesis topics Modeling of an electro-optical system - Design of active optical electro components such as optical phase shifter, modulators and switches based on ring resonator or Mach-Zehnder – Design of complex photonic architectures - Characterization of photonic components - Optical sensors (eg integrated optical gyroscopes based on Sagnac effect) - Optical communications – Quantum Photonics
Company location and place of work Studio di Micorelettronica - STMicroelectronics – Via Ferrata, 4 – Pavia; STMicroelectronics – Via Tolomeo, 1 – Cornaredo (MI)
Time length of the internship - 12 MONTHS
Benefits provided by the company (at least reimbursement of 500€ per month): Reimbursement: 600€ per month; ST shuttle service to reach the place of work; Lunch included at the ST canteen.
Specific company requests
Other comments

Unipv LM+

Progetto Laurea Magistrale Plus

(Students enrolled for the first time in the Academic Year 2017/18, undertaking the internship in the company in 2018/19)

University infos

Laurea degree LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING
University tutor / Thesis supervisor - Piero Malcovati
Courses of the university tutor: Industrial Measurements, Electrical Industrial Measurements, Microsensors, Integrated Microsystems and MEMS Competences of the university tutor: Analog and mixed-signal integrated circuits, Sensor interface circuits, Data converters, Power electronics and power management

Company infos

Company name - STMicroelectronics srl
Company Tutor(s) - Giona Fucili / Maurizio Nessi
Role in the company of the tutor(s) - Designer Engineers

Contents and infos on project and internship

Project title - Analog design for Power Combo
Activity scenario and targets of the internship - Area/Department/office/lab (where the trainee will be involved): *Design of one or more microelectronic circuits to be applied in the HDD, SSD, or Printer fields. These products include Power Management Circuits (Regulators, Motor Drivers), Analog and Mixed-Signal Circuits (D/A, A/D, Supervisory Functions, OpAmp with various requirements up to 5Gb data rate in pre-amp devices). The used technologies are BCD or BiCMOS.*
Background / Expertize of the student required for the internship *A good basic knowledge of electronics even at transistor level (Bipolar, CMOS) is essential. Knowledge of Motor and Regulator Driver, experience in Microelectronics Layout, knowledge of Cadence Virtuoso and Spice like simulators are preferred skills.*
Potential thesis topics Design one or more circuit that will be part of a HDD/SSD/Printer project.
Company location and place of work Via Tolomeo, 1 - 20010 Cornaredo (Mi), Italy.
Time length of the internship - 12 MONTHS
Benefits provided by the company (at least reimbursement of 500€ per month) 600 Euro/month Free company canteen Free shuttle buses
Specific company requests
Other comments

Unipv LM+

Progetto Laurea Magistrale Plus

(Students enrolled for the first time in the Academic Year 2017/18, undertaking the internship in the company in 2018/19)

University infos

Laurea degree LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING
University tutor / Thesis supervisor - Prof. Favalli - Prof. Merlo. The thesis supervisor will be one of them.
Courses / Expertize of the university tutor Merlo - Courses: Elettronica1, Optoelettronica biomedica, MEMS; Competence areas: Photonics MEMS, MOEMS. Favalli - Courses Sistemi di Telecomunicazioni, Wireless Networks, Internet and Multimedia, Wired and Wireless Communications Systems. Competence areas: IP networks, Wireless networks, Video coding and transmission.

Company infos

Company name: TIM - Italtel
Company Tutor(s) - TIM: Marco Schiano; Italtel: Paolo Comi
Role in the company of the tutor(s) - Marco Schiano: Project Manager; Paolo Comi: Research and Innovation Manager

Contents and infos on project and internship

Project title - TIM: Software Defined Optical Networks; Italtel: Softwarized Network Control Layer

Activity scenario and targets of the internship - Area/Department/office/lab (where the trainee will be involved)
TIM department: IP, Transport and Core networks Italtel department: Software BU

The TIM-Italtel internship aims at providing the student good competence level in many layers of modern ICT networks, from optical fiber transport technologies and SDN (Software Defined Networking) control of IP networks to NFV (Network Function Virtualization) softwarized Network Control Layer Applications.

Objectives (TIM):
- To reinforce the student know-how on telecommunications optical technologies and on T-SDN optical networks by a review of theoretical concepts followed by lab experiments;
- To introduce the student to TSDN applied research by developing a plug-in of ONOS network operating system.

Activities:
- Optical fibres
- Passive components
- Optical amplifiers
- DWDM transmission systems
- Intensity Modulation-Direct Detection (IM-DD) transceivers
- Coherent transceivers
- IM-DD and coherent transmission degradation models
- Optical networks
- IP and optical layers integration
- SDN networks
- ONOS plugin development

Objectives (Italtel):
- To provide the student the basic concepts of management, Quality of Service (QoS) and security in ICT networks;
- To introduce the most prominent network and service virtualization techniques, with both commercial and open source solutions.

Activities:
- IP networks and their use in the telecommunications
- Network Management
- Quality of Service (QoS) and Service Level Agreement (SLA)
- Cybersecurity aspects
- Cloud computing and its implementations in open source and commercial solutions in an industrial research environmemt
- Network Function Virtualization (NFV)
- Software Defined Networking (SDN) for IP networks control and programmability
- Network Control Layer Applications
- Traditional telecommunication applications and services
- Novel services and applications in telecommunication networks

Background / Expertize of the student required for the internship TIM - ability to study English technical literature and to carry out effective synthesis; - basic knowledge of fibre optics and optical transmission systems (intensity modulation direct detection receivers and transmitters); - Attitude to the use of numerical simulation tools (the familiarity with the Matlab environment is preferred). Italtel - ability to study English technical literature and to carry out effective synthesis; - basic knowledge of IP networks; - basic knowledge of telecommunication networks; - attitude to teamwork; - basic knowledge of Java or Pyton programming languages is welcome but not mandatory.
Potential thesis topics TIM: Software defined control of optical networks Italtel: Softwarization of telecommunication networks
Company location and place of work Telecom Italia: Torino, via Reiss Romoli, 274 Italtel: via Reiss Romoli, Località Castelletto 20019 - Settimo Milanese (MI)
Time length of the internship - 6 months in Telecom Italia and 6 months in Italtel
Benefits provided by the company (at least reimbursement of 500€ per month) Telecom Italia: 500€ per month scholarship - Italtel: 500€ per month scholarship
Specific company requests
Other comments